

Lawrence Rauchwerger

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Education

Ph.D. in Computer Science, University of Illinois at Urbana-Champaign, 1995.

Ph.D. Thesis: *Run-Time Parallelization: A Framework for Parallel Computation*.

Thesis advisor: David Padua.

M.S. in Electrical Engineering, Stanford University, 1987.

M.S. Research Area: Manufacturing Science and Technology for VLSI (Equipment Modeling).

Engineer in Electronics and Telecommunications, Polytechnic Institute,

Department of Electronic Engineering, 1980, Bucharest, Romania.

Diploma Project: Design and Implementation of an Alphanumeric and Graphic Display.

Research Interests

Compilers for parallel and distributed computing

Parallel and distributed C++ libraries.

Adaptive runtime optimizations.

Architectures for parallel computing.

Awards

NSF Faculty Early Career Development (CAREER) Award, 1998–2002.

Elected Member, International Federation of Information Processing (IFIP), WG3.10, 2003.

TEES Fellow, College of Engineering, Texas A&M University 2002-2003.

TEES Fellow, College of Engineering, Texas A&M University 2005-2006.

TEES Select Young Faculty Award, College of Engineering, Texas A&M University 2000-2001

(awarded to two junior faculty each year by the College of Engineering).

Best student paper award, co-authored with Silviu Rus, Int. Conference on Supercomputing, New York, NY, 2002.

Best student paper award, co-authored with Steve Saunders, Workshop on Performance Optimization for High-level Languages and Libraries, New York, NY, June 2002.

Intel Foundation Graduate Fellowship, 1994.

NASA (Langley) High Performance Computing Consortium (HPC) Graduate Fellowship, 1994.

Experience

Professor, Department of Computer Science, Texas A&M University. (9/06 – present)

Co-Director, PARASOL Laboratory (3/98 – present)

Texas A&M University High Performance Computing Steering Committee. (1999 – present)

Visiting Professor, INRIA Futurs, Orsay, France. (9/04 – 11/04, 7/06 – 8/06)
 IBM T. J. Watson Research Center, Yorktown Heights, NY. (10/03 – 8/04)

Associate Professor, Department of Computer Science, Texas A&M University. (9/01 – 8/06)

Assistant Professor, Department of Computer Science, Texas A&M University. (8/96 – 08/31/01)

Visiting Scientist, AT&T Research Laboratories, Murray Hill, NJ. (6/96-8/96)

Visiting Assistant Professor, Center for Supercomputing R&D, University of Illinois. (9/95-5/96)

Research Assistant, Center for Supercomputing R&D, University of Illinois. (1/89-5/92, 1/94-5/94)

Teaching Assistant, Computer Science Department, University of Illinois. (1/93-12/93)

Summer Intern, IBM T.J. Watson Research Center, Yorktown Heights, NY. (Summer 1992)

Research Assistant, Center for Integrated Systems, Stanford University. (1986–1988)

R & D Engineer, Varian Associates Inc., Thin Film Technology Division, R&D, Palo Alto, CA. (1984–1985)

Design Engineer, Beckman Instruments Inc., Scientific Instruments Division, Irvine, CA. (1983-1984)

Design Engineer, The Felix Computer Company, R. & D. Department, Bucharest, Romania. (1980–1982)

Research Grants

“Adaptive Parallel Processing for Dynamic Applications” *The National Science Foundation* (CAREER Program) (CCR-9734471), PI: L. Rauchwerger, \$237,000, (includes \$10,000 in REU Supplements, 1999, \$27,000 matching supplement, 2000.) June 1, 1998 – May 31, 2004.

“CRS–AES: Collaborative Research: SoftCheck: Compiler and Run-Time Technology for Efficient Fault Detection and Correction in Low nm-Scale Multicore Chips,” *The National Science Foundation* PIs: Maria Garzaran (UIUC) and L. Rauchwerger \$200,000, August 2006 – July 2008.

“STAPL: A High Productivity Parallel Programming Infrastructure,” *Intel Corporation*, PI: L. Rauchwerger, \$30,000, November 03, 2005.

“SmartApps: Middle-ware for Adaptive Applications on Reconfigurable Platforms,” *The Department of Energy, Office of Science (Operating/Runtime Systems for Extreme Scale Scientific Computation Program)*, PI: L. Rauchwerger, co-PIs: M. Adams (Nuclear Engineering), N. Amato, B. Stroustrup, \$1,500,000 September 1, 2004 – August 31, 2007.

“ITR/NGS: STAPL: A Software Infrastructure for Computational Biology and Physics” (ACI-0326350), *The National Science Foundation (Medium ITR Program)*, PI: L. Rauchwerger, co-PIs: N. Amato, B. Stroustrup, M. Adams (Nuclear Engineering), \$416,000, November 1, 2003 – October 31, 2007.

“Efficient Massively Parallel Adaptive Algorithm for Time-Dependent Transport on Arbitrary Spatial Grids,” *The Department of Energy*, PI: M. Adams (Nuclear Engineering), co-PIs: N. Amato, P. Nelson, L. Rauchwerger, \$1,668,827, May 1, 2002 – March 31, 2006.

“Geometry Connectivity and Simulation of Cortical Networks”, *Texas Higher Education Coordinating Board*, PI: N. Amato co-PI: L. Rauchwerger \$240,000 January 1, 2002 - August 31, 2004.

“ITR/SY: Smart Apps: An Application Centric Approach to Scientific Computing” , *The National Science Foundation* (ACR-0113971), PI: L. Rauchwerger, co-PI: N. Amato, \$463,809, September 1, 2001 – August 31, 2005.

- “ITR/AP: A Motion Planning Approach to Protein Folding Simulation”, *The National Science Foundation* (CCR-0113974), PI:N. Amato, co-PI: L. Rauchwerger, \$318,000, September 1, 2001 – August 31, 2005.
- “SmartApps: Smart Applications for Heterogeneous Computing,” (EIA-9975018), *The National Science Foundation (Next Generation Software Program)*, PI: L. Rauchwerger, co-PI: N. Amato, J. Torrellas (Univ. Illinois at Urbana-Champaign), \$610,000 October 1, 1999 – August 31, 2003.
- “PARASOL: An Adaptive Framework for Parallel Processing” (ACI-9872126), *The National Science Foundation*, PI: L. Rauchwerger, co-PI: N. Amato, \$199,662, January 1, 1999 – December 31, 2002.
- “Efficient Massively-Parallel Implementation of Modern Deterministic Transport Calculations” (B347886), *Department of Energy (ASCI ASAP Level 2 and 3 Programs)*, PI: M. Adams (Nuclear Engineering), co-PIs: N. Amato, P. Nelson, L. Rauchwerger, \$889,000, October 21, 1998 – March 31, 2002.
- “Parallel Algorithms for Graph Cycle Detection,” *Sandia National Laboratory*, PI: L. Rauchwerger, \$93,448, September 1, 1999 – January 15, 2002.
- “Develop the How-to of a Qualified Compiler and Linker”, *Aerospace Vehicle Space Institute (AVSI)*, PI: L. Rauchwerger, March 01, 2001 – January 31, 2002. \$45,500,

Fellowship, Equipment, and Software Grants

- ”CRI: A Cluster Testbed for Experimental Research in High Performance Computing” *The National Science Foundation*, PI: V. Taylor co-PI: N. Amato, L. Rauchwerger, \$537,000, May 15, 2006 – April 30, 2008.
- “Workshop NGS: Support for the Workshop on Languages and Compilers for Parallel Computing (LCPC),” *The National Science Foundation*, PI: Lawrence Rauchwerger, Co-PI: Nancy M. Amato, \$15,000, September 1, 2003 – August 31, 2004.
- “MRI: Development of Brain Tissue Scanner,” *The National Science Foundation*, PI: B. McCormick, co-PIs: N. Amato, J. Fallon (UCI), L. Rauchwerger, \$105,000 + \$153,000 funds from Texas A&M. September 1, 2000–July 31, 2001.
- “Education/Research Equipment Grant – HP V-class Shared Memory Multiprocessor Upgrade,” *Hewlett-Packard*, PI: Lawrence Rauchwerger and Nancy Amato, May 2000, approximately \$580,000.
- “Research Equipment Grant – 16 Processor V-class Shared Memory Multiprocessor Server,” *Hewlett-Packard Co.*, PI: L. Bhuyan, co-PIs: N. Amato, L. Rauchwerger, \$1,200,000, 1998.
- “Fellowships in Robotics, Training Science, Mobil Computing and High Performance Computing” (P200A80305), *U.S. Department of Education (GAANN Fellowship Program)*, PI: R. Volz, co-PIs: N. Amato, L. Everett, J. Welch, co-Investigators: L. Rauchwerger, J. Trinkle, N. Vaidya, J. Yen, Texas A&M University, \$601,224, August 15, 1998 – August 14, 2001.

Professional Service & Activities

NSF Panelist

September 1998, October 1998, June 1999, November 2000, May 2002.

Editorial Board Member

Int. Journal of Parallel Processing (IJPP), since 2003.

Guest Editor:

Journal of Parallel Computing, Special Issue on *Parallel Processing for Irregular Applications*, 2000.

Int. Journal of Parallel Computing, 2000, Special Issue on Selected Papers from ICS’99.

Int. Journal of Parallel Computing, 2002, Special Issue on Selected Papers from IWACT’2001.

Program Chair

16th Int. Conf. on Parallel Architectures and Compilation Techniques (PACT), 2007.

16th Workshop on Languages and Compilers for Parallel Computing (LCPC), 2003.

Program Committee Member:

Int. Conf. for High Performance Computing and Communications (SC07), 2007.

Int. Parallel and Distributed Processing Symp. (IPDPS), 2002, 2006, 2007.

Int. W-shop on High-Level Parallel Programming Models and Supportive Environments(HIPS), 2007.

ACM Int. Conf. on Supercomputing (ICS), 2000, 2006, 2007.

Int. Conf. on High-Performance Embedded Architectures and Compilers (HiPEAC), Belgium, 2007.

Int. Conf. on High Performance Computing (HiPC), India, 2000, 2003, 2007.

Int. Conf. on Computer Design (ICCD), 2006.

Int. Conf. on High Performance Computing and Communications (HPCC), 2006.

ACM Int. Conf. on Computing Frontiers, Italy, 2006.

Int. IEEE W-shop on High Performance Computational Biology (HICOMB), 2005;

Int. Conf. on High Performance Computing and Communications (HPCC-05), Italy, 2005;

Workshop on Languages and Compilers for Parallel Computing (LCPC), 2002, 2004, 2005;

Workshop on Patterns in High Performance Computing, Champaign, IL, 2005;

ACM SIGPLAN Symp. Principles and Practice of Parallel Programming (PPoPP), 2005;

High Performance Computer Architecture Conf. (HPCA), 2001, 2002, 2004;

Int. Symp. on Parallel Architectures, Algorithms and Networks (I-SPAN), Philippines, 2002;

ACM Int. Conf. on Supercomputing (ICS'00), Santa Fe, NM, May 2000;

Int. Conf. on Parallel Processing (ICPP), 1999, 2000;

Int. Conf. on Compiler Construction (CC), 1999, 2000;

Int. Conf. on Parallel Architecture and Compilation Techniques (PACT), 1999;

First Workshop on Parallel Computing for Irregular Applications, Orlando, FL, January 1999;

Workshop and Publications Chair:

High Performance Computer Architecture Conf. (HPCA-6), Toulouse, France, January 2000.

Exhibits Chair:

ACM Int. Conf. on Supercomputing (ICS'02), New York, NY, June 2002.

Referee for Scientific Journals and Conferences.

Member IEEE, ACM and IFIP WG3.10.

Significant University and Departmental Service and Activities

Texas A&M University High Performance Computing Steering Committee, 1999 – present.

Senator, Faculty Senate, Texas A&M University, 2001–2005.

Faculty Search Committee, 2002–2003, 2004–2005, 2006–2007.

Department Head Search Committee, 2001–2002.

Endowed Chair Search Committee, 2001–2002.

Computer Engineering Committee, 2002-2003.

Graduate Advisory Committee (GAC), 2001–2002, 2006–2007.

Colloquium Committee. 1998–1999, 1999–2000, 2001–2002 (Chair). 2002–2003 (Chair).

Advisory Committee 2001-2002.

Computer Services Advisory Committee, 1997–1998.

Graduate Admissions and Awards Committee, 2000–2001, 2004–2005, 2006–2007.
Library Committee. 1998–1999, 1999–2000 (Chair).
Total Quality Management (TQM). 1997–1998.

Courses Taught

Graduate:

CPSC-605: Advanced Compiler Design (Fall 96, 97, 98, 99, 00, 01, 02; Spring 05, 07)
CPSC-614: Computer Architecture (Spring 03)
CPSC-654: Supercomputing (Spring 99, 01)
CPSC-681: Graduate Seminar (Spring 07)
CPSC-689: Advanced Topics in Compiler Design (Spring 00, 02, 03)
CPSC-689: Special Topics: Runtime Systems for Parallel Computing (Spring 06)

Undergraduate:

CPSC-434: Compiler Design (Spring 97, 98, 99, 00, 01, 02, 05, 06)
CPSC-481: Undergraduate Seminar (Spring 07)

Student Research Supervision

Graduated PhD Students

Silvius Rus, Ph.D. December 2006, “Hybrid Analysis and its Application to Dynamic Compiler Optimization” Current position: Google, Mountain View, CA.
Hao Yu, Ph.D. August 2004, “Run-time Optimizations of Adaptive Irregular Applications.” Current position: Postdoc, IBM T.J. Watson Research Center, Yorktown Heights, NY
Ye Zhang, Ph.D. (UIUC) May 1999, (co-advised with Prof. Josep Torrellas, University of Illinois), “Hardware for Speculative Run-time Parallelization in Distributed Shared-Memory Multiprocessors”, Current position: Software Engineer, Oracle Corporation, CA.

Graduated Masters Students

Devang Patel, M.S. August 1998, “Compiler Integration of Speculative Run-Time Parallelization.” Current position: Software Engineer, Apple Computer, Sunnyvale, CA.
Francisco Arzu, M.S. Summer 2000, “STAPL: Standard Templates Adaptive Parallel Library.” Current position: Consultant and partner, ClinicalWeb.com, Austin, TX
Julio Carvallo De Ochoa, M.S., Summer 2000, “Parallelization of Loops with Recurrence and Unknown Iteration Space”, Current position: Software Engineer, Wayne Industries, Austin, TX.
William McLendon III, M.S., Fall 2001, “Parallel Detection and Elimination of Strongly Connected Components for Radiation and Transport Sweeps”, Current position: Software Engineer, Scalable Computing Systems Dept., Sandia National Laboratory, Albuquerque, NM.
Mothi Mohan Ram Thoppae, M.S. (EE), Fall 2001, “Hardware and Software Co-techniques for Branch Prediction”, Current position: Component Design Engineer, Intel Corporation, Santa Clara, CA.
Timmie Smith, M.C.S., Summer 2002, Current Position: Ph.D. Student, Texas A&M University, Dept. of Computer Science.
Steven Saunders, M.S., Spring 2003, “A Parallel Communication Infrastructure for STAPL”, Current Position: Software Engineer, Raytheon, Dallas, TX.

Current Graduate Students

Francis Dang, research area: Speculative Techniques, SmartApps.

Alin Jula, research area: Parallel C++ library, parallel dynamic memory management.

Marinus Pennings, research area: Parallelizing Compilers, run-time optimization and compilation.

Antoni Pop, research area: Run-time systems, Operating Systems for SmartApps and STAPL.

Nageswar Rao, research area: Run-time systems, Operating Systems for SmartApps and STAPL.

Ioannis Papadopoulos, research area: Operating Systems for SmartApps and STAPL.

Androniki Pazarloglu research area: Compilers.

Timmie G. Smith, research area: Parallel C++ Library, Parallel Memory Management.

Gabriel Tanase, research area: Parallel C++ Library,

Nathan Thomas, research area: Parallel C++ Library.

Tao Huang, research area: Parallel C++ Library.

Undergraduate Research Projects

William Harris, Purdue University, Speculative Parallelization, Summer 06.

Aditya Awasthi, IIT, India, Summer 06, STAPL.

Saransh Mittal, IIT, India, Summer 06, STAPL.

Carson Brownle, Summer 2005, CS REU Program. Visualization tool for graphs.

Anna Tikhonova, Summer 2005, CRA-W DMP Program, Parallel algorithms in STAPL.

Armando Solar, Nuclear radiation transport simulation. 01/01 – 07/03.

Current Position: PhD student, UC Berkeley

Reshma Ananthakrishnan, Test suite for STAPL, 04/01 – 05/04.

Current Position: Microsoft, Redmond, WA

Andrew Cox, Software Branch Prediction, 9/00 - 5/01. Current Position: Microsoft, Redmond, WA

Steven Saunders, Java Parallel Library, 1/00 - 12/00. Current Position: Raytheon, Dallas, TX

Carrie Searcey, Java Parallel Library, 5/00 - 8/00. Current Position: IBM, Raleigh, NC

Michael Peter, Hardware for speculative run-time parallelization, 1/99-7/99.

Current Position: PhD student, TU Dresden, Germany.

Francis Dang, Run-time parallelization (CPSC 485 project), 6/98 - 6/99.

Current Position: Supercomputing Center, Texas A&M

William McLendon, Performance Monitoring (CPSC 485 project), 6/98 - 6/99.

Current Position: Sandia National Labs, Albuquerque, NM.

Timmie Smith, STAPL: Standard Parallel Adaptive C++ Library, (CPSC 485 project) 7/99 - 12/99.

Current Position: PhD student. Texas A&M.

Invited Presentations (Selected, last 5 years)

“Automatic Parallelization with Hybrid Analysis”,

IBM, T.J. Watson, Yorktown Heights, NY, April, 2005.

HP, Cupertino, CA, Feb. 2006

SIAM Conf. on Computational Science and Engineering, San Francisco, CA, February, 2006.

Compiler & Architecture Int. Seminar, IBM Haifa Research Labs, Haifa, Israel, December, 2005.

Fudan University, Shanghai, China, December, 2005.

- “Efficient Massively Parallel Adaptive Algorithms for Time-Dependent Transport on Arbitrary Grids.”
SIAM Conf. on Computational Science and Engineering, San Francisco, CA, February, 2006.
- “SmartApps: Middleware for Adaptive Applications on Reconfigurable Platforms”,
FAST-OS PI Meeting/Workshop, Rockville, MD, June, 2005.
- “STAPL: A High Productivity Programming Infrastructure for Parallel & Distributed Computing”,
Workshop on Patterns in High Performance Computing, Urbana, IL, May, 2005.
2005 SIAM Conf. on Computational Science and Engineering, Orlando, FL, February, 2005.
- “SmartApps: Adaptive Applications for High Productivity / High Performance”,
UPC, Barcelona, Spain, December, 2004
Technical University, Delft, The Netherlands, November, 2004
Workshop on Scalable Approaches to High Performance and High Productivity Computing, Bertinoro
Int. Center for Informatics (ScalPerf04), Italy, September 2004.
Universita di Pisa, Italy, November, 2004.
INRIA, Paris, France, 2004.
IBM, T.J. Watson, Yorktown Heights, NY, 2004.
- “STAPL: A High Productivity Programming Infrastructure for Parallel and Distributed Computing”,
Workshop on Domain Specific Languages for Numerical Optimization Argonne National Laboratory,
August 18-20, 2004.
IFIP WG3.10, London, UK, February, 2004.
- “Memory Consistency Issues in STAPL”,
DAGSTUHL Seminar: Hardware and Software Consistency Models: Programmability and Performance,
Schloss Dagstuhl, Wadern, Germany, October 2003.
- “Hybrid Analysis”,
DAGSTUHL Seminar: Emerging Technologies: Can Optimization Technology meet their Demands?,
Schloss Dagstuhl, Wadern, Germany, February 2003.
- “Compiler-Assisted Software and Hardware Support for Reduction Operations”,
NSF Next Generation Software Workshop, Fort Lauderdale, FL, April 2002.
- “STAPL: An Adaptive, Generic Parallel C++ Library”,
NSF Workshop on Software for the IBM Blue Gene Architecture, IBM T.J. Watson Research Center,
April, 2002.
- “Removing Architectural Bottlenecks to the Scalability of Speculative Parallelization”,
IBM Research, Haifa, Israel, July 2001.
- “SmartApps: An Application Centric Approach to High Performance Computing”,
Workshop for Next Generation Software, San Francisco, CA, April, 2001.

Publications in Refereed Journals, Conferences and Workshops

(Organized by topic; most papers available at <http://parasol.tamu.edu/~rwerger/>)

Compilers

- [1] A. Jula and L. Rauchwerger “Custom Memory Allocation for Free: Improving Data Locality with Container-Centric Memory Allocation,” in *Proc. of the 19-th Workshop on Languages and Compilers for Parallel Computing (LCPC)*, New Orleans, Louisiana, Nov 2006, to appear.

- [2] S. Rus, G. He and L. Rauchwerger, “Scalable Array SSA and Array Data Flow Analysis”, in *Proc. of the 18-th Workshop on Languages and Compilers for Parallel Computing (LCPC)*, Hawthorne, NY, 2005. *Lecture Notes in Computer Science (LNCS)*, Springer-Verlag, to appear.
- [3] S. Rus, G. He, C. Alias and L. Rauchwerger, “Region Array SSA”, in *Proc. of the 15-th Int. Conf. on Parallel Architecture and Compilation Techniques (PACT)*, Seattle, WA, 2006.
- [4] Hao Yu, Lawrence Rauchwerger, “An Adaptive Algorithm Selection Framework for Reduction Parallelization”, *IEEE Transactions on Parallel and Distributed Systems*, **17** (19),2006, pp. 1084–1096.
- [5] H. Yu, D. Zhang and L. Rauchwerger, “An Adaptive Algorithm Selection Framework”, in *Proc. of the 13th Int. Conf. on Parallel Architecture and Compilation Techniques (PACT)*, Antibes Juan-les-Pins, France, October, 2004, pp. 278–289.
- [6] S. Rus, D. Zhang and L. Rauchwerger, “The Value Evolution Graph and its Use in Memory Reference Analysis”, in *Proc. of the 13th Int. Conf. on Parallel Architecture and Compilation Techniques (PACT)*, Antibes Juan-les-Pins, France, October, 2004, pp. 243–254.
- [7] S. Rus, D. Zhang and L. Rauchwerger, “Automatic Parallelization Using the Value Evolution Graph”, in *Proc. of the 17-th Workshop on Languages and Compilers for Parallel Computing (LCPC)*, West Lafayette, IN, 2004. Also in *Lecture Notes in Computer Science (LNCS)*, **3602**, Springer-Verlag, 2005, pp. 379–393.
- [8] S. Rus, D. Zhang and L. Rauchwerger, “The Value Evolution Graph and its Use in Memory Reference Analysis”, in *Proc. of the 11-th Workshop on Compilers for Parallel Computing (CPC)*, Seon Monastery, Chiemsee, Germany, 2004, pp. 175–186. Invited Paper.
- [9] S. Rus, L. Rauchwerger and J. Hoefflinger, “Hybrid Analysis: Static & Dynamic Memory Reference Analysis”, in *Int. Journal of Parallel Programming*, Special Issue, **31**(4), 2003, pp. 251–283.
- [10] H. Yu, F. Dang, and L. Rauchwerger, “Parallel Reductions: An Application of Adaptive Algorithm Selection”, *Proc. of the 15-th Workshop on Languages and Compilers for Parallel Computing (LCPC)*, Washington, DC., July, 2002. Also in *Lecture Notes in Computer Science (LNCS)*, Springer-Verlag, **2481**, 2005, pp. 188–202.
- [11] S. Rus, L. Rauchwerger and J. Hoefflinger, “Hybrid Analysis: Static & Dynamic Memory Reference Analysis”, in *Proc. of the ACM 16-th Int. Conf. on Supercomputing (ICS02)*, New York, NY, June 2002, pp. 274–284. **Best Student Paper Award.**
- [12] F. Dang, H. Yu and L. Rauchwerger, “The R-LRPD Test: Speculative Parallelization of Partially Parallel Loops”, in *Proc. of the Int. Parallel and Distributed Processing Symposium (IPDPS2002)*, Fort Lauderdale, FL, April 2002, pp. 20–30.
- [13] L. Rauchwerger, N.M. Amato and J. Torrellas, “SmartApps: An Application Centric Approach to High Performance Computing”, in *Proc. of the 13th Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, Yorktown Heights, NY, August 2000. Also in *Lecture Notes in Computer Science*, **2017**, Springer-Verlag, 2000, pp. 82–96.
- [14] F. Dang and L. Rauchwerger, “Speculative Parallelization of Partially Parallel Loops”, in *Proc. of the 5-th Workshop on Languages, Compilers, and Run-time Systems for Scalable Computers (LCR2000)*, Rochester, NY, May 2000. Also in *Lecture Notes in Computer Science*, **1915**, 2000, pp. 285–299.

- [15] H. Yu and L. Rauchwerger, “Adaptive Reduction Parallelization”, in *Proc. of the ACM 14-th Int. Conf. on Supercomputing, (ICS’00)*, Santa Fe, NM, May 2000, pp. 66–77.
- [16] H. Yu and L. Rauchwerger, “Techniques for Reducing the Overhead of Run-time Parallelization”, in *Proc. of the 9th Int. Conf. on Compiler Construction (CC’00)*, Berlin, Germany, March 2000, Lecture Notes in Computer Science, **1781**, Springer-Verlag, 2000, pp. 232–248.
- [17] L. Rauchwerger and D. Padua, “The LRPD Test: Speculative Run-Time Parallelization of Loops with Privatization and Reduction Parallelization,” *IEEE Transactions on Parallel and Distributed Systems*, Special Issue on Compilers and Languages for Parallel and Distributed Computers, **10**(2), 1999, pp. 160–180.
- [18] H. Yu and L. Rauchwerger, “Run-time Parallelization Optimization Techniques”, in *Proc. of the 12th Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, August 1999, San Diego, CA. Also in Lecture Notes in Computer Science, **1863**, Springer-Verlag, 2000, pp. 481–484.
- [19] D. Patel and L. Rauchwerger, “Implementation Issues of Loop-level Speculative Run-time Parallelization”, *Proc. of the 8th Int. Conf. on Compiler Construction (CC’99)*, Amsterdam, The Netherlands, March 1999. *Lecture Notes in Computer Science*, **1575**, Springer-Verlag, 1998, pp. 183–197.
- [20] Lawrence Rauchwerger, “Run-Time Parallelization: It’s Time Has Come”, *Journal of Parallel Computing*, Special Issue on Languages & Compilers for Parallel Computers, **24**(3–4), 1998, pp. 527–556.
- [21] D. Patel and L. Rauchwerger, “Principles of Speculative Run-time Parallelization”, *Proc. of the 11th Annual Workshop on Languages and Compilers for Parallel Computing (LCPC)*, August 1998, Chapel Hill, NC. Also in Lecture Notes in Computer Science, **1656**, Springer-Verlag, 1998, pp. 323–337.
- [22] W. Blume, R. Doallo, R. Eigenmann, J. Grout, J. Hoeflinger, T. Lawrence, J. Lee, D. Padua, Y. Paek, W. Pottenger, L. Rauchwerger, and P. Tu, “Advanced Program Restructuring for High-Performance Computers with Polaris,” *IEEE Computer*, **29**(12), 1996, pp. 78–82.
- [23] W. Blume, R. Eigenmann, K. Faigin, J. Grout, J. Lee, T. Lawrence, J. Hoeflinger, D. Padua, Y. Paek, P. Petersen, B. Pottenger, L. Rauchwerger, P. Tu, and S. Weatherford, “Restructuring Programs for High-Speed Computers with Polaris”, *Proc. of the 1996 ICPP Workshop on Challenges for Parallel Processing*, August 1996, pp. 149–162.
- [24] L. Rauchwerger, N.M. Amato and D. Padua, “A Scalable Method for Run-Time Loop Parallelization,” *Int. Journal of Parallel Programming*, **23**(6), 1995, pp. 537–576. (CSRD Tech. Rept. 1400.)
- [25] L. Rauchwerger, N.M. Amato and D. Padua, “Run-Time Methods for Parallelizing Partially Parallel Loops,” *Proc. of the 9th ACM Int. Conf. on Supercomputing (ICS’95)*, July 1995, Barcelona, Spain, pp. 137–146.
- [26] L. Rauchwerger and D. Padua, “The LRPD Test: Speculative Run-Time Parallelization of Loops with Privatization and Reduction Parallelization,” *Proc. of the ACM SIGPLAN 1995 Conf. on Programming Language Design and Implementation (PLDI95)*, June 1995, La Jolla, CA., pp. 218–232.
- [27] L. Rauchwerger and D. Padua, “Parallelizing While Loops for Multiprocessor Systems,” *Proc. of the 9th Int. Parallel Processing Symposium*, April 1995, Santa Barbara, CA, pp. 347–356.

- [28] L. Rauchwerger and D. Padua, “The Privatizing DOALL Test: A Run-Time Technique for DOALL Loop Identification and Array Privatization,” *Proc. 8th ACM Int. Conf. on Supercomputing*, July 1994, Manchester, England, pp. 33–43.
- [29] W. Blume, R. Eigenmann, J. Hoeflinger, D. Padua, P. Petersen, L. Rauchwerger and P. Tu, “Automatic Detection of Parallelism: A Grand Challenge for High-Performance Computing,” *IEEE Parallel and Distributed Technology, Systems and Applications - Special Issue on High Performance Fortran*, Fall 1994, **2**(3), pp. 37–47.
- [30] W. Blume, R. Eigenmann, K. Faigin, J. Grout, J. Hoeflinger, D. Padua, P. Petersen, B. Pottenger, L. Rauchwerger, P. Tu, and S. Weatherford, “Polaris: Improving the Effectiveness of Parallelizing Compilers,” *Proc. 7th Ann. Workshop on Languages and Compilers for Parallel Computing (LCPC)*, August 1994, Ithaca, New York; Also in *Lecture Notes in Computer Science*, **892**, Springer-Verlag, 1994, pp. 141–154.
- [31] L. Rauchwerger and D. Padua, “Run-Time Methods for Parallelizing DO Loops,” *Proc. of the 2nd Int. Workshop on Massive Parallelism: Hardware, Software and Applications*, October 1994, Capri, Italy, pp. 1–15.

Parallel Libraries & Applications

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