Architecture Interaction with Databases (II)

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CS533
Memory System Characterization of Commercial Workloads
Barroso et al, ISCA-98
Workloads

• OLTP
  – banking system: transactions update balance in randomly-selected account
  – small computation
  – 4 tables updated per transaction --> I/O

• DSS
  – read-only queries
  – more complicated
  – queries can be parallelized

• Web index search
  – similar to DSS
  – read only
Experiments

• Hardware platform:
  – Server with 4 300-MHz processors
  – latency to mem: 260ns
  – hardware event counters

• Simulator platform:
  – SimOS: simulates app+os
Monitoring Results

• Breakdown of execution time (Figs 3 and 4):
  – CPI of OLTP is very high --> poor performance
  – OLTP:
    • L3 misses (see table 2): workload overwhelms caches
    • Also important: L1 and L2 misses (that hit in L3)
    • dirty misses (data fetched from another cache): 15%, which are slower:
      – 417ns to get data from another cache vs 267ns to get data from memory
      – dirty misses increase with the number of processors and L3 size
  – DSS:
    • More efficient: lower CPI
    • L1 misses, since L1 not fully successful at keeping the working set
    • L2 can hold the state
    • no dirty misses
  – Altavista: best performance
Simulation Results

- L1-D and L1-I 32 KB caches
- unified 2 MB L2
Simulation Results

- Sharing Patterns of OLTP (fig 5)
  - User time dominates
  - benefits from larger/more assoc caches
  - Cache and memory stall still important
  - L2 cache behavior for different cache sizes/assoc (Fig 5)
  - Most communication misses due to true (not F) sharing
  - Analyzing the number processors (Fig 6). IF P goes up:
    - increases the hit time
    - ratio of true to false sharing does not change.
    - Overall: communication misses
Cache Sizes

- Larger on-chip caches good for DSS and OLTP (Fig 6)
- Larger on-chip caches cache most misses in DSS
- OLTP has large footprint: continue to benefit with 4-8MB L2
Sensitivity to Cache Line Size

- Changing line size of the L3 (Fig 8)
  - data communicated among processors (true sharing) has good spatial locality
  - Cold misses also spatial locality
  - No impact on replacement misses
Summary

• OS and I/O do not dominate tuned DB
• OLTP:
  – I and D locality only captured with large L3 caches
  – high communication miss rate (dirty misses)
• DSS and AltaVista:
  – Sensitive to the size and latency of L1
  – Less sensitive to off chip caches sizes/latencies
• Workloads require different server designs