Prefetching (II):
Using Processors-In-Memory (PIM) for Prefetching

Instructor: Josep Torrellas
CS533

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Memory Stall Time

Execution of non-dependent instructions

Main Proc [stall]

$+Mem
Intelligent Memory

**User-Level Memory Thread (ULMT)**

How to use ULMT to improve memory performance?

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Exploiting Intelligent Memory

ULMT for Memory-Side Prefetching
Correlation Prefetching

- Records sequences of miss addresses in a correlation table
- When the head of a sequence is seen, prefetch the rest
- Effective: if miss sequences repeat

1. \[ a[4*(i++)] \]

2. \[ a[\text{foo}(i)] \]
   \[ a[b[i]] \]

3. \[ &A \rightarrow &B \rightarrow &C \rightarrow ... \rightarrow &Z \]

4. List/Tree/Graph with arbitrary but fixed traversal order
Correlation Prefetching

- Effective for irregular+regular apps
- Needs little info: cache miss addresses
- No compiler support
- Works with existing binaries
- How to implement the correlation table?
  - Past work: Expensive hardware
    - Few MBs of on-chip SRAM for the table (larger than cache!)
    - Table size has to scale with app working set
  - Paper proposes: Software
    - Is software fast enough? Yes.
Communication Mechanism

Processor chip

Main Proc

L1 $

L2 $

Memory Controller

North Bridge Chip

Interconnect

Memory chip

Mem Proc

L1 $

DRAM Cells

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Timeline of the Prefetch Handler

- Miss address obtained
- Prefetch addresses produced
- Prefetcher free

<table>
<thead>
<tr>
<th>Prefetching phase</th>
<th>Learning phase</th>
</tr>
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</table>

Response time

Occupancy time

- **Ideal algorithm:**
  - lowest response time
  - occupancy time < time between misses

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Correlation Table

Basic Organization [1]

Addr of immediate successors

Tag Succ_L1

NumSucc = 2

Advanced Organization

Addr of next immediate successors

Tag Succ_L1 Succ_L2 ...

NumSucc = 2

NumLevels = n

[1] Joseph & Grunwald, ISCA 97
Learning Phase

Basic Organization

<table>
<thead>
<tr>
<th>Tag</th>
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</tr>
</thead>
<tbody>
<tr>
<td>A</td>
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Current miss

A, B, C, A, D, C, ...

Advanced Organization

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Prefetching Phase

Basic Organization
On miss A

Chaining

Basic: 1 miss ⇒ *immediate successor*
- no far ahead prefetching
- low coverage and late prefetches

Basic + Chaining:
- low accuracy
- high response time

Advanced Organization
On miss A

Advanced: 1 miss ⇒ *several succ levels:*
+ far ahead prefetching
+ high coverage
+ timely prefetches
+ high accuracy
+ low response time
Simulation Environment

- **Main processor:**
  - 1.6 GHz, 6-issue OOO
  - L1: 2-way 16 KB; L2: 4-way 512 KB
  - Mem: 243 cycle RT

- **Memory processor:**
  - 800 MHz, 2-issue OOO
  - L1: 2-way 32 KB
  - Mem: 100 cycle RT (in NorthBridge), 56 cycle RT (in DRAM)

- **Correlation table:**
  - Application dependent, e.g. 64K entries, 3 levels, 2 successors

- **Applications**
  - Specint2000, Specfp2000, NAS, Olden
Predictability of miss sequences

- Can predict miss sequences accurately

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Execution Time (Mem Proc in DRAM)

- Busy
- L1 to L2
- Beyond L2

N: No Prefetch
S: Sequential
B: Basic
A: Advanced
+: S + advanced
Customization

Normalized Execution Time

Busy L1 to L2 Beyond L2

N: No Prefetch
+: S + advanced
C: Customization

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Cycles Between Misses

- Occupancy time of prefetch thread must be < 200 cycles
Thread Response and Occupancy Time

- All algo feasible: Occupancy Time < 200 cycles
- Advanced/Repl has the best Response Time
DRAM vs. Mem Controller Chip
Prefetching Effectiveness
Bus Utilization

- **Advanced**: avg increase of 8%